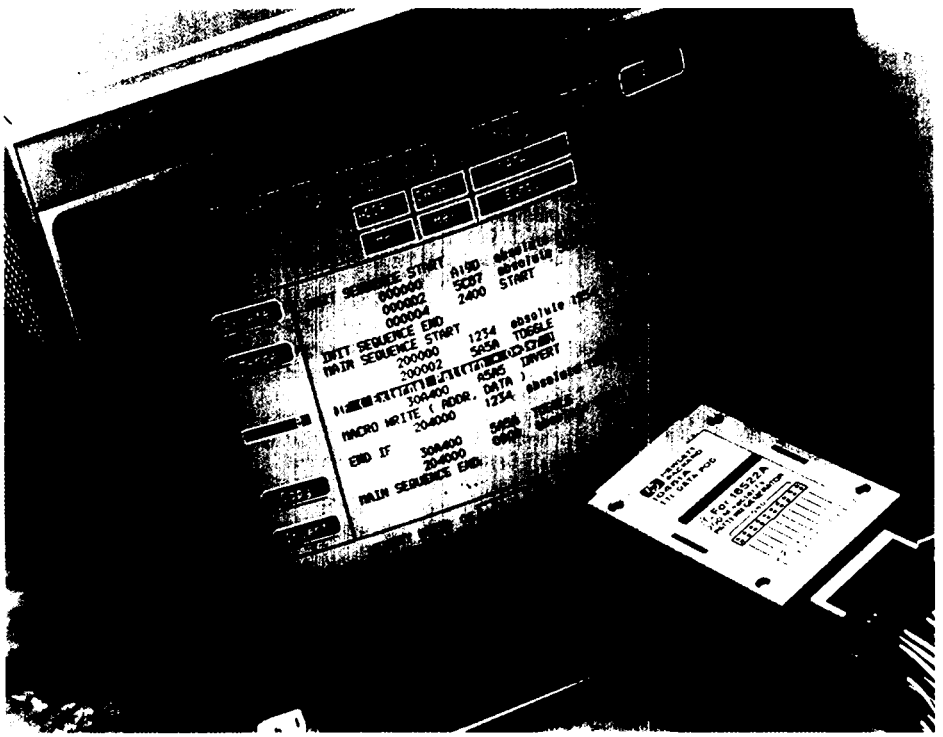
HP 16522A

- 200 million vectors-per-second—20 bits/module
- 100 million vectors-per-second 40 bits/module
- 258,048 vector deep memory
- Up to 200 output channels in a 5-module system



HP 16522A Digital Pattern Generator Module

Functionally Test Your Designs

The HP 16522A digital pattern generator module is the perfect tool for functional testing of your digital design. The pattern generator allows you to check the functional characteristics of your system. See how your system responds to specific signals or clock speeds. Correlate data captured with other HP 16500 series modules to verify correct operation. Use the HP 16522A in automated test environments to run design verification tests quickly, using only one instrument. Save time normally spent developing custom test hardware used for stimulus.

Use Parallel Development of Subsystems to Reduce Time to Market

When you have the ability to test system subcomponents, you can find problems earlier in the design process. As a result, you can cut your development time and make improvements in the finished product. Use the HP 16522A as a substitute for missing boards, integrated circuits (ICs), or buses. Instead of waiting for the missing pieces, you can continue to test and verify your design.

Software engineers can create infrequently-encountered test conditions and verify that their code works—before complete hardware is available. Hardware engineers can generate the patterns necessary to put their circuit in the desired state, operate the circuit at full speed or single-step the circuit through a series of states.

Digital Stimulus and Response

Configure the HP 16500C system to provide both stimulus and response in a single instrument. For example, have the pattern generator stimulate a circuit initialization sequence. The pattern generator can then signal the state or timing analyzer to begin making measurements. Use compare mode on the state analyzer to determine if the circuit or subsystem is functioning as expected.

Conveniently enter patterns in hex, octal, binary, decimal, two's complement, or symbolic bases. Easily edit data with Delete, Insert, Copy, and Merge functions. Use macros to specify repeating patterns, without reentering them.

Digital Stimulus for Prototype Turn-on and Evaluation

The HP 16522A pattern generator provides a number of features to help you turn on and evaluate prototypes quickly:

Vectors Up to 200 Bits Wide

Vectors are defined as a "row" of labeled data values. Each data value can be from one to 32-bits wide. Each vector is output on the rising edge of the clock. Up to five, 40-channel HP 16522A modules can be interconnected within an HP 16500C (or HP 16501A expansion frame) to support vectors of any width up to 200 bits with excellent channel-to-channel skew characteristics (see specific data pod information on the facing page). At clock speeds above 100 MHz, the pattern generator operates in "half channel" mode, resulting in 20 output channels per HP 16522A module.

Synchronized Clock Output

You can operate with either an internal or external clock. The external clock is input via a clock pod, and has no minimum frequency or duty cycle requirements. The internal clock is selected as a clock period from 5 ns to 250 μs in a 1, 2, 2.5, 4, 5, 8 sequence (4 kHz to 200 MHz). A Clock Out signal is available from the clock pod and can be used as an edge strobe with a variable delay of up to 11 ns.

Wait for Input Pattern

The clock pod also accepts a 3-bit level-sensed input pattern. Up to four "Wait for Pattern" conditions can be defined and inserted any number of times into a stimulus program. A "Wait for IMB" (intermodule measurement bus) condition can also be defined to wait for an intermodule measurement bus event.

Initialize Block for Repetitive Patterns

The vectors in the initialize block are only output during the first occurrence of a repetitive run. This feature is very useful when the circuit or subsystem needs to be initialized. A "Signal IMB" instruction can be inserted to signal other modules to start acquisition at the time "interesting activity" is started.

Pattern Generator Module (cont'd)

HP 16522A

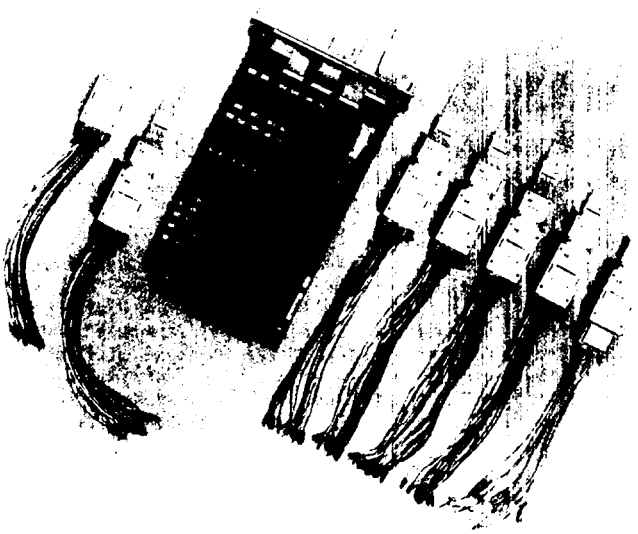
Conditional Branch at 50 MHz
With clock speeds of 50 MHz or less, a single "IF block" of vectors can be defined. The "IF condition" can be either a 3-bit input pattern or an IMB event. When running repetitively, use of the "IF" instruction will result in a latency time of indeterminate duration between the last and the first vectors of the main sequence.

Macros and Repeat Loops Simplify Creation of Stimulus Programs
Parameterized macros permit you to define a pattern sequence once, and then insert the macro by name wherever it is needed. Repeat loops enable you to repeat a defined block of vectors a specified number of times. A memory utilization indicator helps you track the percentage of memory used in the stimulus program.

ASCII Input File Format
The HP 16522A supports an ASCII file format which facilitates connectivity to other tools in your design environment. By generating stimulus vectors in this file format, you can read stimulus programs into the pattern generator via the HP 16500C LAN (Local Area Network) connection, via the HP 16500C HP-IB connection, or via the HP 16500C floppy disk drive. This format has been specifically designed for fast file transfer into the HP 16522A pattern generator.

Configuration
The HP 16522A requires a single slot in an HP 16500B/C or 16501A frame (The pattern generator is not compatible with the HP 16500A frame). The pattern generator is designed for operation with the external clock and data pods and lead sets described on this page. Both the data pods and data cables use standard connectors that you can design into your system.

The electrical characteristics of the data cables are also described for users with specialized applications who want to avoid the use of a data pod.



Up to five HP 16522A 40-channel pattern generator modules can be interconnected into a 200 channel system. The clock and data pods support TTL, CMOS, 3.3 volt, and ECL logic levels.

Lead Set Characteristics

HP 10474A 8-Channel Probe Lead Set: Provides most cost-effective lead set for the HP 16522A clock and data pods. IC clips are not included.
HP 10347A 8-Channel Probe Lead Set: Provides 50 Ω coaxial lead set for unterminated signals, required for HP 10465A ECL Data Pod (unterminated). IC clips are not included.

Data Pod Characteristics

HP 10461A TTL Data Pod
Output Type: 10H125 with 100 Ω series
Maximum Clock: 200 MHz
Skew (Note 1): Typical < 2 ns; worst case = 4 ns
Recommended Lead Set: HP 10474A

HP 10462A 3-State TTL/CMOS Data Pod
Output Type: 74ACT11244 with 100 Ω series; 10H125 on non-3-state channel 7 (Note 2)
3-State Enable Pin: High input disables output; low input or no connect enable output
Maximum Clock: 100 MHz
Skew (Note 1): Typical < 4 ns : worst case = 12 ns
Recommended Lead Set: HP 10474A

HP 10464A ECL Data Pod (terminated)
Output Type: 10H115 with 330 Ω pulldown, 47 Ω series
Maximum Clock: 200 MHz
Skew (Note 1): Typical < 1 ns; worst case = 2 ns
Recommended Lead Set: HP 10474A

HP 10465A ECL Data Pod (unterminated)
Output Type: 10H115 (no termination)
Maximum Clock: 200 MHz
Skew (Note 1): Typical < 1 ns; worst case = 2 ns
Recommended Lead Set: HP 10347A

HP 10466A 3-State TTL/3.3 Volt Data Pod
Output Type: 74LVT244 with 100 Ω series; 10H125 on non-3-state channel 7 (Note 2)
3-State Enable Pin: High input disables output; low input or no connect enable output
Maximum Clock: 200 MHz
Skew (Note 1): Typical < 3 ns ; worst case = 7 ns
Recommended Lead Set: HP 10474A

Note 1: Typical skew measurements made at pod connector with approximately 10 pF/50 k Ω load to GND; worst-case skew numbers are a calculation of worst-case conditions through circuits. Both numbers apply to any channel within a single or multiple module system.
Note 2: Channel 7 on the 3-state pods is brought out in parallel as a non-3-state signal. By looping this output back into the 3-state enable line, the channel can be used as a 3-state enable.

Data Cable Characteristics Without a Data Pod

The HP 16522A data cables without a data pod provide an ECL terminated (1 k Ω to – 5.2 V) differential signal (from a type 10E156 or 10E154 driver). These are usable when received by a differential receiver, preferably with a 100 Ω termination across the lines. These signals should not be used single-ended due to the slow fall time and shifted voltage threshold (they are not ECL compatible).

Clock Pod Characteristics

HP 10460A TTL Clock Pod
Clock Output Type: 10H125 with 47Ω series; true and inverted
Clock Output Rate: 100 MHz maximum
Clock Out Delay: 11 ns maximum in 9 steps
Clock Input Type: TTL – 10H124
Clock Input Rate: DC to 100 MHz
Pattern Input Type: TTL – 10H124 (no connect is logic 1)
Clock-in to Clock-out: Approximately 30 ns
Pattern-in to Recognition: Approximately 15 ns + 1 clk period
Recommended Lead Set: HP 10474A

HP 10463A ECL Clock Pod
Clock Output Type: 10H116 differential unterminated; and differential with 330 Ω to – 5.2 V and 47 Ω series
Clock Output Rate: 200 MHz maximum
Clock Out Delay: 11 ns maximum in 9 steps
Clock Input Type: ECL – 10H116 with 50 k Ω to –5.2 V
Clock Input Rate: DC to 200 MHz
Pattern Input Type: ECL – 10H116 with 50 k Ω (no connect is logic 0)
Clock-in to Clock-out: Approximately 30 ns
Pattern-in to Recognition: Approximately 15 ns + 1 clk period
Recommended Lead Set: HP 10474A

Key Literature

HP 16522A 200 M Vector/sec Pattern Generator Module for the HP 16500B/C Logic Analysis System, p/n 5964-2250E
Digital Verification with the HP 16522A Pattern Generator, p/n 5964-6347E