

Telecom Circuit Testing

Application Note:



PA-20 PA-25 PFA-30 PFA-35



Summary

Using the powerful features of these testers a comprehensive range of Telecom circuit testing is possible. This makes them ideal for commissioning, maintaining and troubleshooting telecom circuits.

Telecom Circuit Testing

RX/TX mode with Drop and Insert

In RX/TX mode a framed signal is generated internally by the instrument. The transmitter and receiver operate independently. During installation and maintenance of 2Mbit/s circuits a framed signal is often used to simulate normal operating conditions.

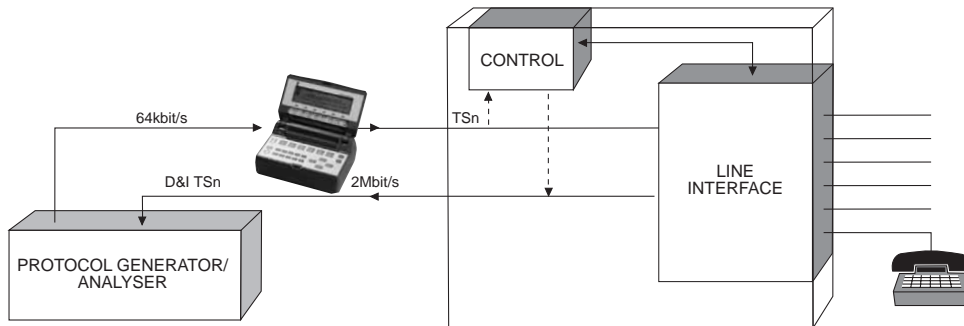
A test pattern can be inserted into one selectable timeslot or $n \times 64\text{kb/s}$ timeslots of the generated signal.

A programmable idle code is used to fill the unoccupied

time-slots. With PCM30 and PCM30 CRC generated framed signals a programmable signalling code can be inserted into timeslot 16 in all channels.

The digital information in any selected timeslot can be dropped to the V.11 interface, and external data from the V.11 interface inserted in its place. In the example below PFA-35 is simulating a network allowing an external protocol generator/analyser to control a PABX.

n.b. Not available on PA-20 or PFA-30



THROUGH mode with n x 64kbit/s Drop and Insert

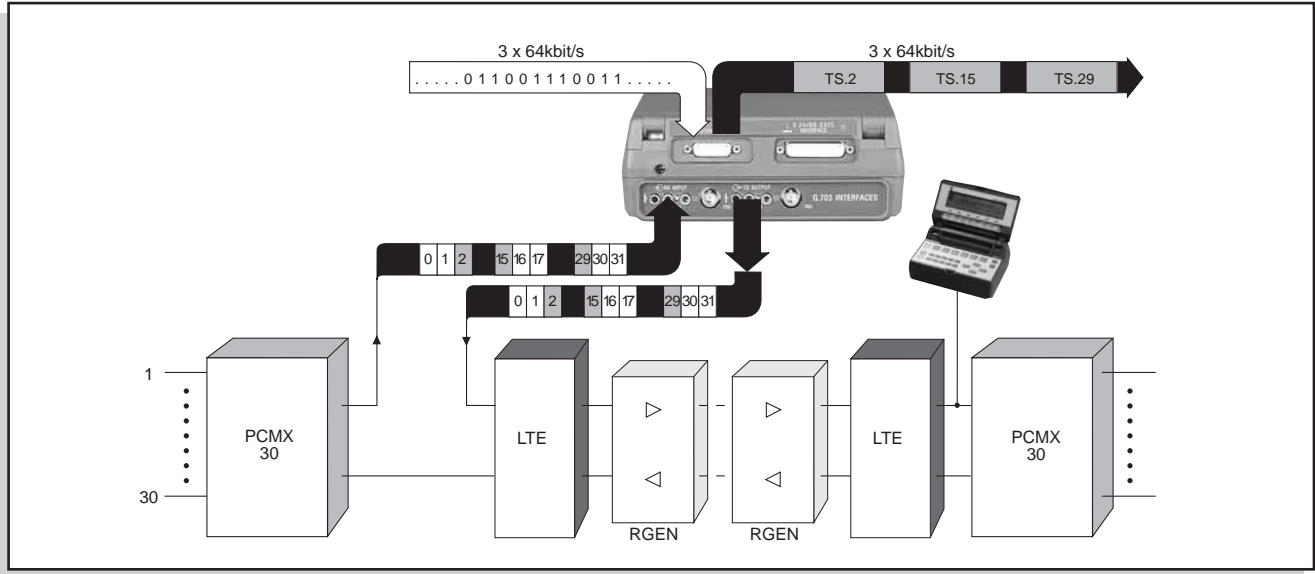
In Through mode the framed signal received by the instrument is connected through to the transmitter. This allows:-

The digital information in any selected timeslot or n x 64kbit/s timeslots of the live signal to be replaced by any selected test pattern.

Alternatively, the digital information in any selected timeslot can be dropped to the V.11 interface, and external data from the V.11 interface inserted in its place.

PA-25 and PFA-35 can drop/insert n x 64kbit/s (n=1-31) timeslots to the V.11 interface.

n.b. Not available on PA-20 or PFA-30



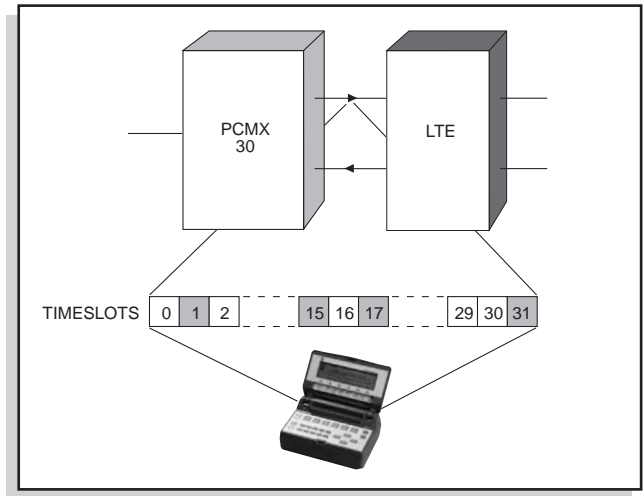
Error and Alarm analysis

LEDs provide an instant indication of error and alarm status of the network under test. Time analysis of errors and alarms is provided using histograms.

All error performance parameters are evaluated in accordance with CCITT Rec G.821.

BER/BLER and G.821 analysis of a prbs in one or n x 64 kbit/s selectable timeslots

Transmitting data in n x 64kbit/s timeslots within a 2Mbit/s frame is becoming increasingly popular. One instrument can be used, for example, to transmit a 256kbit/s test pattern into the multiplexer. This is distributed over 4 x 64kbit/s timeslots within the 2Mbit/s frame. A second instrument evaluates the test pattern in the occupied timeslots at monitor points down the line and displays any errors and alarms detected in a numeric and graphical format. Any combination of timeslots up to n = 31 can be used.



BER and G.821 analysis using the CRC or FAS information in the 2Mbit/s frame

The frame alignment signal (FAS) consists of a defined pattern of bits. This signal can be monitored for bit errors. Similarly the CRC word can be monitored for bit errors.

These are both simple methods of making a BER and G.821 performance analysis of a live circuit. A time analysis of these errors is available as a histogram.

In addition the PA-25 and PFA-35 display the FAS word error ratio.

Current test	1		
Error free secs	82	97.61904%	Summary
Error secs	2	2.38095%	
Sev errored secs	0	0.00000%	
Degraded mins	0	0.00000%	
Available time	84	67.74193%	
Unavailable time	40	32.25806%	
Menu	Alarm	Hist	-more-
		Reset	Stop

Frame and timeslot digital word monitoring

Valuable information, such as the alarm status of a frame is indicated by the digital frame words. These words are monitored and the FAS, NFAS, MFAS and NMFAS frame words displayed on the instrument screen. The digital octet in any selected timeslot is also displayed.

Frains	PCM30C			00000000
Time slot	2 (C2)	Data	0010 0001	
Frame no.	0	FAS	1001 1011	
FAS	1001 1011	MFAS	0000 1011	
NFAS	0101 1111	CRC MFAS	0010 1111	
S Bits	+1	-1	Edit	Freeze

S_a-bit monitoring and generation

Use of the S-bits in the NFAS word of a 2Mbit/s frame structure is being introduced worldwide for maintenance of ISDN PRA circuits. These bits carry loop commands to the remote end and status reports from the remote end. PA-25 and PFA-35 can individually set and monitor the S_a-bits in the NFAS word.

n.b. Not available on PA-20 or PFA-30

NMFAS	1011	NFAS 4-8	*Tx Bits setup*
AD1	0	Bit 4 (Sa)	SMF1 SMF2
E2	1	Bit 5 (Sa)	1001 1111
0	1	Bit 6 (Sa)	1111 1111
		Bit 7 (Sa)	1010 1100
		Bit 8 (Sa)	0000 0000
		Enter	1111 1111

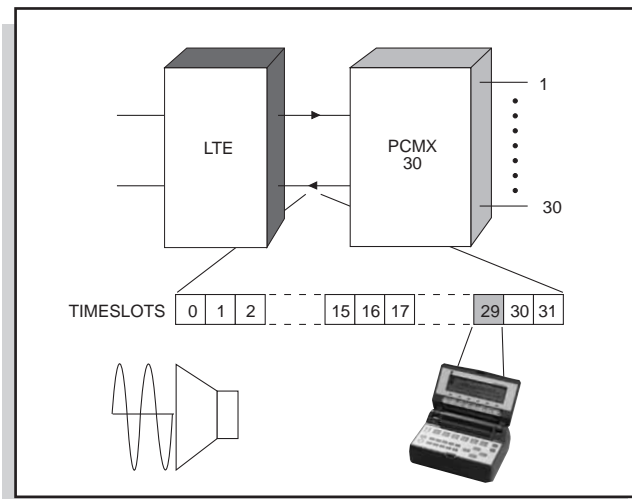
Round trip delay (framed)

Round trip delay measurement is provided on looped back circuits by inserting a pattern in n x 64kbit/s timeslots in a 2Mbit/s frame. All PA-25/PFA-35 test patterns can be used. Maximum delay is 10 seconds and the resolution of the displayed result is +/-1 microsecond. This allows location of remote loops for example.

n.b. Not available on PA-20 or PFA-30

PCM decoding and audio output of a selected timeslot

Audio checks on the digital side of the multiplexer are used as a first line diagnostic test to identify impaired voice channels. The digital information in any selected timeslot can be decoded and output to the instrument's built-in loudspeaker. This can also be used to listen to modem and fax signals.

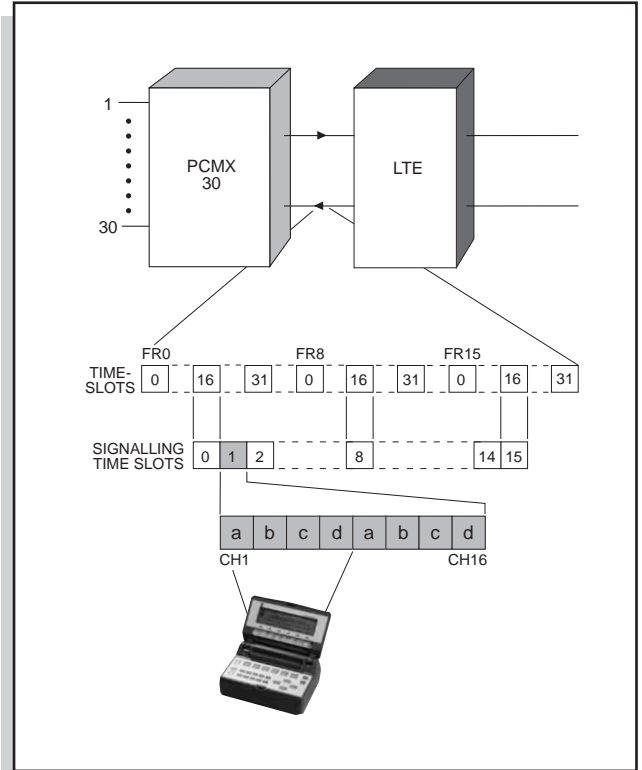


Channel Associated Signalling monitoring

The Channel Associated Signalling status of all 30 telephone channels can be simultaneously monitored and displayed on the instrument screen. This gives an instant indication of which channels are busy. Busy channels are highlighted using inverse video.

In addition the 4-bit Channel Associated Signalling information for any selected telephone channel can be monitored. The current 4-bit code is displayed with up to 15 previous code changes.

For monitoring call sequences the 4-bit signalling code can be printed out as changes occur.



Error Injection

Bit, Code, FAS or CRC errors can be injected either singly or as a ratio.

Error injection allows the user to stress the system under test. PA-25/PFA-35 can also inject Bit, Code, FAS or CRC errors at a selectable, programmable frequency from 0 to 999 per second. The errors are in bursts at the rate of 1kHz.

Frequency offset

The 2Mbit/s internal clock can be offset by +/-150 ppm in 1 ppm steps during framed and unframed operation.

n.b. Not available on PA-20 or PFA-30

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