TLA700 System Specifications

Tables A–18 through A–20 list the specifications common to the TLA715, TLA714, TLA720, and TLA721 logic analyzers. Detailed specifications for the individual logic analyzers begin on page A–23.

Table A- 18: TLA700 Backplane interface

Characteristic	Description
Slots	
Portable mainframe	4
Benchtop mainframe	10 (three slots taken up by the controller module)
Expansion mainframe	13
✓ CLK10 Frequency	10 MHz ±100 PPM
Relative Time Correlation Error[1,2] (Typical)	
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx “MagniVu” data	2 ns
TLA7Axx to TLA7Axx “MagniVu” data	2 ns
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx “MagniVu” data	-3 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an internal clock	1 TLA7Lx/Mx/Nx/Px/Qx sample - 0.5 ns
TLA7Axx to TLA7Axx “normal” data using an internal clock	1 TLA7Axx sample - 0.5 ns
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an internal clock	1 TLA7Lx/Mx/Nx/Px/Qx sample - 0.5 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an external clock	2 ns
TLA7Axx to TLA7Axx “normal” data using an external clock	2 ns
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an external clock	4 ns
TLA7Lx/Mx/Nx/Px/Qx “MagniVu” to DSO data	3 ns
TLA7Axx “MagniVu” to DSO data	2 ns
TLA7Lx/Mx/Nx/Px/Qx to DSO “normal” data using an internal clock[3]	1 TLA7Lx/Mx/Nx/Px/Qx sample + 2 ns
TLA7Axx to DSO “normal” data using an internal clock[3]	1 TLA7Axx sample + 2 ns
TLA7Lx/Mx/Nx/Px/Qx to DSO “normal” data using an external clock[3]	3 ns
TLA7Axx to DSO “normal” data using an external clock[3]	2 ns
DSO to DSO[3]	3 ns

1 Includes typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a “typical” number for the measurement. Assumes standard accessory probes are utilized.

2 For time intervals longer than 1 μs between modules, add 0.01% of the difference between the absolute time measurements to the relative time correlation error to account for the inaccuracy of the CLK10 source.

3 The DSO module time correlation is measured at the maximum sample rate on one channel only.

Table A-19: TLA700 Backplane latencies

Characteristic	Portable mainframe and benchtop mainframe	Expansion mainframe
System trigger and external signal input latencies[2] (Typical)		
External system trigger input to TLA7Lx/Mx/Nx/Px/Qx probe tip[4]	-266 ns	-230 ns
External system trigger input to TLA7Axx probe tip[4]	-653 ns	-617 ns
External signal input to TLA7Lx/Mx/Nx/Px/Qx probe tip via Signal 3, 4[5]	-212 ns + Clk	-176 ns + Clk
External signal input to TLA7Axx probe tip via Signal 3, 4[5]	-212 ns + Clk	-176 ns + Clk
External signal input to TLA7Lx/Mx/Nx/Px/Qx probe tip via Signal 1, 2[5, 6]	-634 ns + Clk	-596 ns + Clk
External signal input to TLA7Axx probe tip via Signal 1, 2[5, 6]	-636 ns + Clk	-615 ns + Clk
External system trigger input to DSO probe tip[4]	-25 ns	11 ns
System trigger and external signal output latencies[1] *(Typical)*		
TLA7Lx/Mx/Nx/Px/Qx probe tip to external system trigger out	376 ns + SMPL	412 ns + SMPL
TLA7Axx probe tip to external system trigger out	794 ns + SMPL	830 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx probe tip to external signal out via Signal 3, 4[3]		
OR function	366 ns + SMPL	402 ns + SMPL
AND function	379 ns + SMPL	415 ns + SMPL
TLA7Axx probe tip to external signal out via Signal 3, 4[3]		
OR function	792 ns + SMPL	828 ns + SMPL
AND function	800 ns + SMPL	836 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx probe tip to external signal out via Signal 1, 2[3,6]		
normal function	364 ns + SMPL	385 ns + SMPL
inverted logic on backplane	364 ns + SMPL	385 ns + SMPL
TLA7Axx probe tip to external signal out via Signal 1, 2[3,6]		
normal function	796 ns + SMPL	817 ns + SMPL
inverted logic on backplane	796 ns + SMPL	817 ns + SMPL

Table A- 19: TLA700 Backplane latencies (Cont.)

Characteristic	Portable mainframe and benchtop mainframe	Expansion mainframe
DSO probe tip to external system trigger out	68 ns	104 ns
DSO Probe tip to external signal out via Signal 3, 4[3]		
OR function	65 ns	101 ns
AND function	75 ns	111 ns
DSO probe tip to external signal out via Signal 1, 2[3,6]		
normal function	68 ns	89 ns
inverted logic on backplane	71 ns	92 ns
Inter-module latencies (Typical)		
TLA7Lx/Mx/Nx/Px/Qx to DSO inter-module system trigger[1,4]	358 ns + SMPL	394 ns + SMPL
TLA7Axx to DSO inter-module system trigger[1,4]	772 ns + SMPL	808 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module system trigger[1,4]	66 ns + SMPL	102 ns + SMPL
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module system trigger[1,4]	479 ns + SMPL	515 ns + SMPL
TLA7Axx to TLA7Axx inter-module system trigger[1,4]	116 ns + SMPL	152 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to DSO inter-module ARM[1]	360 ns + SMPL	396 ns + SMPL
TLA7Axx to DSO inter-module ARM[1]	779 ns + SMPL	815 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM[1,5]	108 ns + SMPL + Clk	144 ns + SMPL + Clk
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM[1,5]	479 ns + SMPL + Clk	533 ns + SMPL + Clk
TLA7Axx to TLA7Axx inter-module ARM[1,5]	111 ns + SMPL + Clk	147 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2[1,5,6]	116 ns + SMPL + Clk	137 ns + SMPL + Clk
TLA7Axx to TLA7Axx inter-module via Signal 1, 2[1,5,6]	113 ns + SMPL + Clk	134 ns + SMPL + Clk
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2[1,5,6]	534 ns + SMPL + Clk	555 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Q to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4[1,5]	116 ns + SMPL + Clk	152 ns + SMPL + Clk
TLA7Axx to TLA7Axx inter-module via Signal 3, 4[1,5]	124 ns + SMPL + Clk	160 ns + SMPL + Clk
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4[1,5]	545 ns + SMPL + Clk	581 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module System Trigger[1,4]	-287 ns + SMPL	-251 ns + SMPL

Table A-19: TLA700 Backplane latencies (Cont.)

Characteristic	Portable mainframe and benchtop mainframe	Expansion mainframe
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module System Trigger[4]	-240 ns	-204 ns
DSO to TLA7Axx inter-module System Trigger[4]	-598 ns	-562 ns
DSO to DSO inter-module System Trigger[4]	50 ns	86 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module ARM[1,5]	-300 ns + SMPL + Clk	-264 ns + SMPL + Clk
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM[5]	-192 ns + Clk	-156 ns + Clk
DSO to TLA7Axx inter-module ARM[5]	-600 ns + Clk	-564 ns + Clk
DSO to DSO inter-module ARM	59 ns	95 ns
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2[5,6]	-179 ns + Clk	-158 ns + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module via Signal 1, 2[1,5,6]	-294 ns + SMPL + Clk	-273 ns + SMPL + Clk
DSO to TLA7Axx inter-module via Signal 1, 2[5,6]	-598ns + Clk	-577 ns + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module via Signal 3, 4[1,5]	-294 ns + SMPL + Clk	-258 ns + SMPL + Clk
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4[5]	-184 ns + Clk	-148 ns + Clk
DSO to TLA7Axx inter-module via Signal 3, 4[5]	-598 ns + Clk	-562 ns + Clk

1 **SMPL represents the time from the event at the probe tip inputs to the next valid data sample of the LA module. In the Normal Internal clock mode, this represents the delta time to the next sample clock. In the MagniVu Internal clock mode, this represents 500 ps or less. In the External clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.**

2 **All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.**

3 **All signal output latencies are validated to the rising edge of an active (true) high output.**

4 **In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.**

5 **"Clk" represents the time to the next master clock at the destination logic analyzer. In the asynchronous (or internal) clock mode, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. In the synchronous (or external) clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.**

6 **Signals 1 and 2 are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.**

Table A-20: TLA700 External signal interface

Characteristic	Description
System Trigger Input	TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Input Levels V_{IH} V_{IL}	TTL compatible input ≥ 2.0 V ≤ 0.8 V
Input destination	System trigger
Input Mode	Falling edge sensitive, latched (active low)
Minimum Pulse Width	12 ns
Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods
Maximum Input Voltage	0 to +5 V peak
External Signal Input	TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Input Destination	Signal 1, 2 Signal 3, 4
Input Levels V_{IH} V_{IL}	TTL compatible input ≥ 2.0 V ≤ 0.8 V
Input Mode	Active (true) low, level sensitive
Input Bandwidth[1] Signal 1, 2 Signal 3, 4	 50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Accepts signals during valid acquisition periods via real-time gating
Maximum Input Voltage	0 to +5 V peak
System Trigger Output	TTL compatible output via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Source selection	System trigger
Source Mode	Active (true) low, falling edge latched
Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output ≥4 V into open circuit ≥ 2 V into 50 Ω to ground ≤ 0.7 V sinking 10 ma
Output Protection	Short-circuit protected (to ground)

Table A-20: TLA700 External signal interface (Cont.)

Characteristic	Description
External Signal Output	TTL compatible outputs via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Source Selection	Signal 1, 2 Signal 3, 4 10 MHz clock
Output Modes Level Sensitive	User definable Active (true) low or active (true) high
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL output ≥ 4 V into open circuit ≥ 2 V into 50 Ω to ground ≤ 0.7 V sinking 10 ma
Output Bandwidth[2] Signal 1, 2 Signal 3, 4	 50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously
Output Protection	Short-circuit protected (to ground)
Intermodule signal line bandwidth	Minimum bandwidth up to which the intermodule signals are specified to operate correctly
Signal 1, 2 Signal 3, 4	50 MHz square wave minimum 10 MHz square wave minimum

1 **The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.**

2 **The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.**